Express Mail No. **EV 346 810 382 US**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Cecile AULNETTE et al.

Application No.:

Filing Date: January 22, 2004

For: SEMICONDUCTOR STRUCTURE FOR PROVIDING STRAINED CRYSTALLINE LAYER ON INSULATOR AND METHOD FOR FABRICATING SAME

Confirmation No.

Group Art Unit:

Examiner:

Atty. Docket No.: 4717-7300

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Pursuant to applicants' duty of disclosure under 37 C.F.R. 1.56, applicants submit herewith twelve (12) references for the Examiner's review and consideration. These references are listed on the enclosed Form PTO-1449.

These references were cited in European Search Reports, copies of which are enclosed. It is respectfully requested that the references be made of record in this application by the Examiner's completion and return of the PTO Form 1449.

No fee or certification is believed to be due for this submission since the references are being submitted concurrent with the filing of this application. Should any fees be required, however, please charge such fees to **Winston & Strawn** Deposit Account No. 50-1814.

Respectfully submitted,

Date: 4/22/04

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Enclosures

NY:835421.1

LIST OF REFERENCES CITED BY APPLICANT
(Use several sheets if necessary)

ATTY. DOCKET NO.:	APPLICATION NO.:
4717-7300	
APPLICANT: Cecile AULNETTE et al.	
FILING DATE: January 22, 2004	GROUP:

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,770,868	6/1998	Gill et al.	257	190	
	AB	6,059,895	5/2000	Chu et al.	148	33.1	
	AC	2002/0017642	2/2002	Mizushima et al.	257	19	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AD	EP 1 253 648	10/2002	European Patent Office	H01L	29/78	X	
	AE	WO 02 15244	2/2002	PCT	H01L	21/205	X	

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AF	Cheng et al., "SiGe-on-Insulator (SGOI): Substrate Preparation and MOSFET Fabrication for Electron Mobility Evaluation," IEEE International SOI Conference, 10/01, pp. 13-14 (2001).
	AG	Colinge, "Silicon-on-Insulator Technology," VLSI, p. 47.
	AH	Huang et al., "Electron and Hole Mobility Enhancement in Strained SOI by Wafer Bonding," *IEEE Transactions on Electron Devices*, vol. 49, no. 9, pp. 1566-71 (Sep. 2002).
	AI	Iyer & Auberton-Herve (ed.), "Silicon Wafer Bonding Technology," EMIS Processing Series No. 1, pp. 22, 36, 57.
	AJ	Li et al., "Investigation of strain relaxation of $Ge_{1-x}Si_x$ epilayers on Ge(001) by high-resolution x-ray reciprocal space mapping," *Semiconductor Science and Technology*, vol. 10, pp. 1621-28 (Dec. 1995).
	AK	Takagi et al, "Device structure and electrical characteristics of strained-Si-on-insulator (strained-SOI) MOSFETs," *Material Science and Engineering*, vol. 89, no. 1-3, pp. 426-434 (Feb. 2002).
	AL	Taraschi et al., "Relaxed SiGe-on-insulator fabricated via wafer bonding and etch back," *J. Vac. Sci. Technol.*, B 20(2), pp. 725-27 (Mar/Apr. 2002).

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with **MPEP 609**; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.